INSTRUCTION DATA

Dowty RFL Industries Inc. ● Boonton, New Jersey

Model 66 CMDEC

COMMAND DECODER CARD

DESCRIPTION

The Model 66 CMDEC is one of the RFL 66 TDMS Series of plug-in modules. This card is the complement of Model 66 CMDGEN and is normally used in a Remote Station to decode and output command pulses depending upon the three-bit command code received. It contains an aperture timer and various input requirements to assure a high degree of security. The 66 CMDEC is suitable for use in Select/Operate, Select/Check/Operate, Direct Operate, Proportional Control, Polled and Non-Polled systems.

SPECIFICATIONS

Ambient Temperature: −30 to +70°C.

Power: 11 to 13 Vdc @ 7 mA.

Size: One standard one-half-inch increment in an RFL 68 Chassis.

PROGRAMMING AND CONNECTION

This module contains CMOS logic circuits and special handling precautions should be observed. Refer to "CMOS Handling Precautions", RFL Document 12175.

TABLE 1

COMMAND	Logic Level at Terminals		
	D	E	C
PT CANCEL	1	1	1
PT SELECT	1	1	0
EXECUTE A	1	0	1
EXECUTE B	1	0	0
EXECUTE C	0	1	1
EXECUTE D	0	1	0
EXECUTE E	0	0	1
EXECUTE F	0	0	0

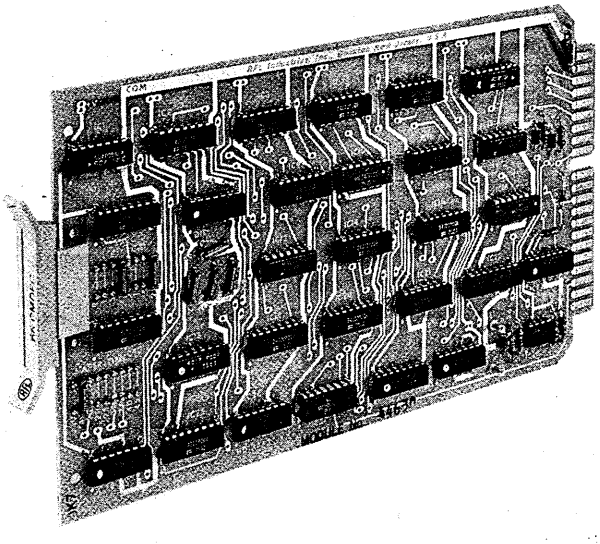


Figure 1. Model 66 CMDEC Command Decoder.

All unused input terminals or unused inputs to integrated circuits must be returned to +V or circuit common.

COMMAND CODE

The received COMMAND CODE which comes from the 66 OREG is connected to Terminals C, E, and D according to Table 1.

$\overline{\text{INHIBIT A}}$
$\overline{\text{INHIBIT B}}$

The $\overline{\text{INHIBIT A}}$ and $\overline{\text{INHIBIT B}}$ inputs are used to inhibit a PT SELECT command if either of these inputs is at a logic 0. This feature may be used to prevent selecting into an execute situation, as in the rare case where the transistor used to drive an execute relay has shorted.

$\overline{\text{UPDATE}}$

Terminal 19, $\overline{\text{UPDATE}}$, is wired to Terminal 7 of the 66 DEC/R. This signal is used to start the command process after new information has arrived and settled in the 66 OREG cards.

MY ADDRESS

Terminal P is used for multi-remote systems; otherwise, for one-on-one systems this terminal should be hard wired to +V. If this terminal has a 0 input when an update occurs, it will cause the 66 OREG cards and the POINT MEMORY to clear and, further, it will terminate any execute pulse which may have been in progress.

CMND MSG OR $\overline{\text{TERMINATE}}$

Terminal 13 must be high when the $\overline{\text{UPDATE}}$ pulse rises from a 0 to 1 and must stay high during the execute commands. If it is not high when $\overline{\text{UPDATE}}$ makes its transition, no execute pulses will be permitted. If Terminal 13 is dropped to a low during the execute pulses, the execute pulses will be immediately terminated. In polled systems it is not unusual to assign one bit in the message to differentiate command messages from other types of messages, and that bit can be wired to Terminal 13.

BDFLG

The BDFLG input at Terminal 17 is wired to BDFLG, Terminal 10, of the 66 OREG card which outputs the COMMAND CODE. If this is not done, then an erroneous message received could either cause an EXECUTE F command or a repeat of the last command received.

PWRFL

Terminal 15, PWRFL, should be connected to Terminal V of the 66 DEC/R. As long as Terminal 15 stays high and for two more seconds after it drops low because the power has returned to normal, the 66 OREG cards and the POINT MEMORY will be held cleared and, further, it will terminate any execute pulse which may have been in progress.

CF

Terminal 14 should be connected to the carrier-detector output of the communications receiver. The 66 OREG cards and POINT MEMORY will be cleared, and any execute pulse which may have been in progress will be terminated for as long as the carrier has failed, but, not less than for 2 seconds. Carrier failure is indicated by a logic one. This terminal has a 12kΩ pull-up resistor and so may be used with open-collector or CMOS tone units. Connect Terminal 14 to common if this feature is not desired.

OUTPUT REGISTER CLEAR

Terminal 16 should be connected to the CLR input, Terminal 11, of the 66 OREG cards.

PERMIT

The PERMIT signal at Terminal 12 is available for the system designer to use as necessary. This output will be high as long as the following conditions are met: MY ADDRESS = 1, CMND MSG = 1, BDFLG = 0, PWRFL = 0, and CF = 0.

PERMIT PULSE

A PERMIT PULSE will be generated at Terminal M each time a valid command is received. It lasts for 0.244 mS.

CMDED

A 0.244 mS pulse will be generated at Terminal H each time an EXECUTE A, B, C or D command is received. This CMDED pulse is useful in some systems to authorize only commanded change-of-states to occur without triggering an alarm.

POINT MEMORY LOAD & CLEAR

Terminal K is connected to the POINT MEMORY load input. Terminal 18 is wired to the POINT MEMORY clear input. It will go high whenever a message is received with someone else's address (and MY ADDRESS = 0), power fails, carrier is lost or a POINT CANCEL PULSE as described below is true.

POINT CANCEL PULSE

A POINT CANCEL PULSE signal causes the POINT MEMORY to be cleared and is also available for the system designer to use as desired. A high going pulse at Terminal 11 will be generated in any of several ways: A received PT CANCEL command will cause a pulse, or, depending upon how the X, Y and Z Jumpers are programmed, so will an aperture time-out or the termination of an EXECUTE A, B, C, or D command.

X, Y, & JUMPERS

If aperture time-out is to cause a point cancel, then the X1 Jumper should be installed; otherwise, install the X0 Jumper. If point cancel after an EXECUTE C or D command is required, then install the Y1 Jumper; otherwise, the Y0 Jumper. If point cancel after an EXECUTE A or B command is required, then install the Z1 Jumper; otherwise, the Z0 Jumper.

The DIRECT/SELECT Jumper should be installed in the DIRECT position for Direct Operate systems or it should be installed in the SELECT position for the Select-type of systems.

APE. OPEN

Terminal X will be high when the aperture is opened. When the DIRECT/SELECT Jumper is in the SELECT position, the aperture can be opened and the timer started only by receipt of a PT SELECT command, but the timer will be restarted by either another PT SELECT command or by an EXECUTE A, B, C or D command. With the DIRECT/SELECT Jumper in the DIRECT position, any of those five commands will start and/or restart the aperture timer.

APERTUF TIME JUMPER

The aperture will stay open for as long as programmed by the APERTURE TIME Jumper. If the aperture timer is not to be used, the APERTURE TIME Jumper should be installed in the 0 position. The aperture can also be closed by receipt of a PT CANCEL command, carrier loss, power failure, bad data, CMND MSG = 0 or MY ADDRESS = 0.

EXECUTE PULSES

The actual execute pulses come out where shown on the right hand side of the schematic. Pulse duration for the EXECUTE A–B pair is controlled by placement of the EXECUTE A OR B DURATION Jumpers and likewise for the EXECUTE C–D pair. The EXECUTE E and EXECUTE F pulses are fixed at 0.244 mS each.

EXECUTE DURATIO JUMPERS

THEORY OF OPERATION

Timing and pulse widths are developed from an 8192 Hz oscillator made of IC30, IC12B and their associated resistors and capacitor located at area (B5) on Figure 3. The oscillator has a period of 0.122 mS, and this clock signal is available at IC12B-6 for use elsewhere on the module. IC29B and IC29A each multiply the period twice, and a 0.488 mS clock is available at IC29A-1. IC28 further multiplies the period by 10 for use in the aperture timer.

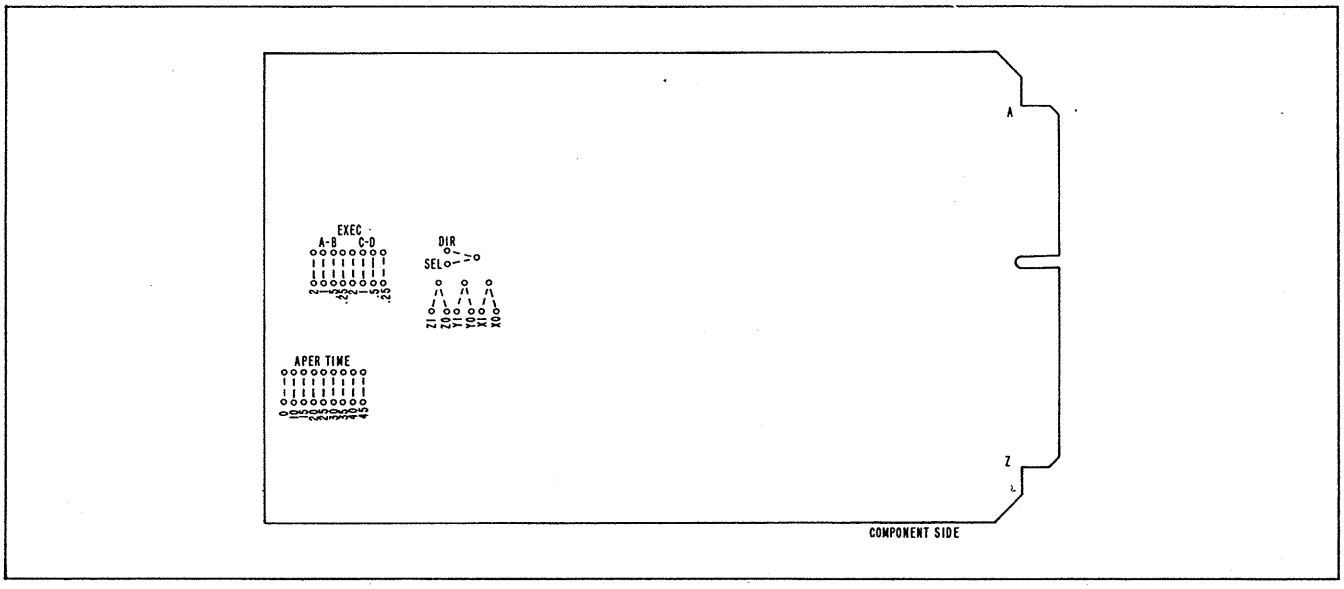


Figure 2. Location of jumpers for programming, Model 66 CMDEC.

IC6 (A3) is a BCD-to-decimal decoder. Only one of its output lines will be high for a given input code. The six EXECUTE lines are taken over to the right side of the schematic where they are gated with various pulses to be described later. PT SELECT is gated with the INHIBIT inputs in IC12C (B3) and then gated with the PERMIT PULSE in IC10C (E2), which, in turn, will cause a POINT MEMORY LOAD PULSE and also open the aperture. PT CANCEL is gated with the PERMIT PULSE in IC11A (C2); from there it passes through IC13C (D2) and IC14A (D1) to output a POINT CANCEL PULSE, output a POINT MEMORY CLEAR signal and reset the aperture.

The PERMIT PULSE is developed in IC22B and IC23A, both at (C2). It will be generated if PERMIT is true when $\overline{\text{UPDATE}}$ goes from a logic 0 to a logic 1. If PERMIT is true, IC23A-5 will be low, and $\overline{\text{UPDATE}}$ will clock a 1 to the $\overline{Q}$ output. The next 0.122 mS CLK pulse will cause IC22B-5 to go high, and, the next 0.122 mS CLK pulse will leave both IC22B-5 and IC22B-4 high. With IC22B-4 at a logic 1, IC23A will be set, and IC23A-2 will be low, so that the following 0.122 mS CLK pulse will leave IC22B-5 at 0. Thus, the PERMIT PULSE will last for two 0.122 mS periods or 0.244 mS. PERMIT PULSE is available at Terminal M (D1).

PERMIT is the signal which essentially means everything is OK to allow a command to take place. When PERMIT is true, IC13A-9 (B2) will be low which can only be so if all three inputs to IC13A are at a logic 0. MY ADDRESS and CMND MSG must both be highs to keep IC16C-10 (A2) and IC13A-8 low. BDFLG must equal zero, and the output of IC16B (B1) must be low, which, of course, means that both of its inputs must be highs. IC16B-6 is normally high except for a momentary pulse when $\overline{\text{UPDATE}}$ goes high if MY ADDRESS is false. IC16B-5 is also normally high except when PWRFL or CF equal a logic one or the 2-second timer is in process.

The momentary pulse at IC16B-6 referred to in the above paragraph comes from IC23B-13 (A2). If MY ADDRESS = 0 when $\overline{\text{UPDATE}}$ makes the 0 to 1 transition, that 0 will be transferred from IC23B-9 to IC23B-13 and a logic 1 will appear at Pin 12. It will then take two 0.122 mS CLK pulses to make IC22A-12 (B2) high and set IC23B again.

IC20 (B1) counts 0.488 mS CLK pulses to create a 2-second delay. If CF = 1, the logic causes IC21D-11 (B1) to stay low for the duration of the carrier failure or for 2 seconds, whichever is longer. If PWRFL = 1, the logic will cause IC21D-11 to stay low for the duration of the power failure plus 2 more seconds.

The 2-second timer exists to prevent any message which may be in transit when the carrier or power fails from being misinterpreted and so causing any erroneous control action. It also protects against flip-flops being in unknown states when the power comes up.

A logic 1 at Terminal 14 (A1) sets the flip-flop made of IC21C/IC21D (B1) and holds IC21D-11 low. Lows at the input of IC15-B (B1) remove the reset on IC20. Even if CF returns to a 0 and likewise IC21D-12, then IC21D-11 can not return high until IC20-2 goes high and resets the flip-flop. If CF = 1 longer than 2 seconds, IC20-2 will lock up at a high because IC15D will prevent further clocking. The high stays there until CF drops and the IC21C/IC21D flip-flop can be reset and in turn reset IC20. The PWRFL signal causes an identical action except that the IC20 reset signal is maintained through IC15B while PWRFL = 1.

The aperture circuit is found in the upper right-hand corner of the schematic, (FGH1). The aperture is opened and the timer started or restarted by a high

going pulse at IC9B-4 (E2). This pulse will reset IC19 (F1), IC18 (G1), the flip-flop made of IC1C/IC2C (H1), and it will set IC24A (G1). IC1C-10 (H1) will be high, and IC19 will be free to count 4.88 mS CLK pulses.

The output of IC27D will cycle high every five seconds. After the proper number of 5-second periods, depending upon the APERTURE TIME Jumper, IC24A-3 (G1) will go high and clock a 1 into IC24A-2. The next time the 0.122 mS CLK drops low (approximately 60 μS later), IC24B will clock the high over to its Q output. When IC24B-13 goes high, it sets the IC1C/IC2C flip-flop, sets IC24A, will cause a POINT CANCEL PULSE if Jumper X1 (D2) is installed and it sets IC23A (C2). With IC1C-10 at a 0, additional clock pulses will be prevented from getting to IC19 (F1) by IC16A (E1).

The inverter IC27-E (G2), flip-flop IC24B, and the OR gate IC13B (C2) are necessary to insure that aperture time out and PERMIT PULSE do not occur at the same time.

The aperture timer can always be started or restarted by a PT SELECT command. The decoded command and PERMIT PULSE are gated together at IC10C (E2). When both are true, IC10C-10 will be low forcing IC10B-4 (E2) high which will cause IC9B-4 (E2) to be a high.

With the DIRECT/SELECT Jumper (C4) in the DIRECT position, IC4D-11 (D4) will be held high so that a decoded EXECUTE A or B command from IC4C (C3) which is gated with PERMIT PULSE in IC3C can be passed through IC3D (D3), then IC4A to IC9B. Decoded EXECUTE C or D commands are gated in a similar fashion. Thus for Direct Operate systems, any of those four commands will start or restart the aperture timer.

With the DIRECT/SELECT Jumper in the SELECT position, the aperture must be opened in order for the four decoded commands EXECUTE A, B, C or D to get beyond the IC3A and IC3D gates (D3). When the aperture is opened IC27F-15 (H1) will be low and so will both inputs to IC2C (D4). IC2C-10 will be high and, therefore, so will IC4D-11. When the aperture is closed, IC2C-8 will be high, and IC2C-10 will be low. With both inputs to IC4D as lows, its ourput will be low, and the signals are blocked from passing through IC3A and IC3D.

The EXECUTE A or B DURATION is timed in IC17 (E4). If the decoded command gets beyond IC3D, then IC8B-9 (E4) will be high during the time PERMIT PULSE is high. The 0.122 mS pulse will cause the Q output of IC8B to follow its D input, and so Pin 13 will follow the PERMIT PULSE, but displaced 0.122 mS in time. When IC8B-13 goes high, it resets IC17 and the flip-flop made of IC1A (F3) and IC2B. IC1A-9 will be high and the proper command will be permitted through IC11C (H3) or IC11D.

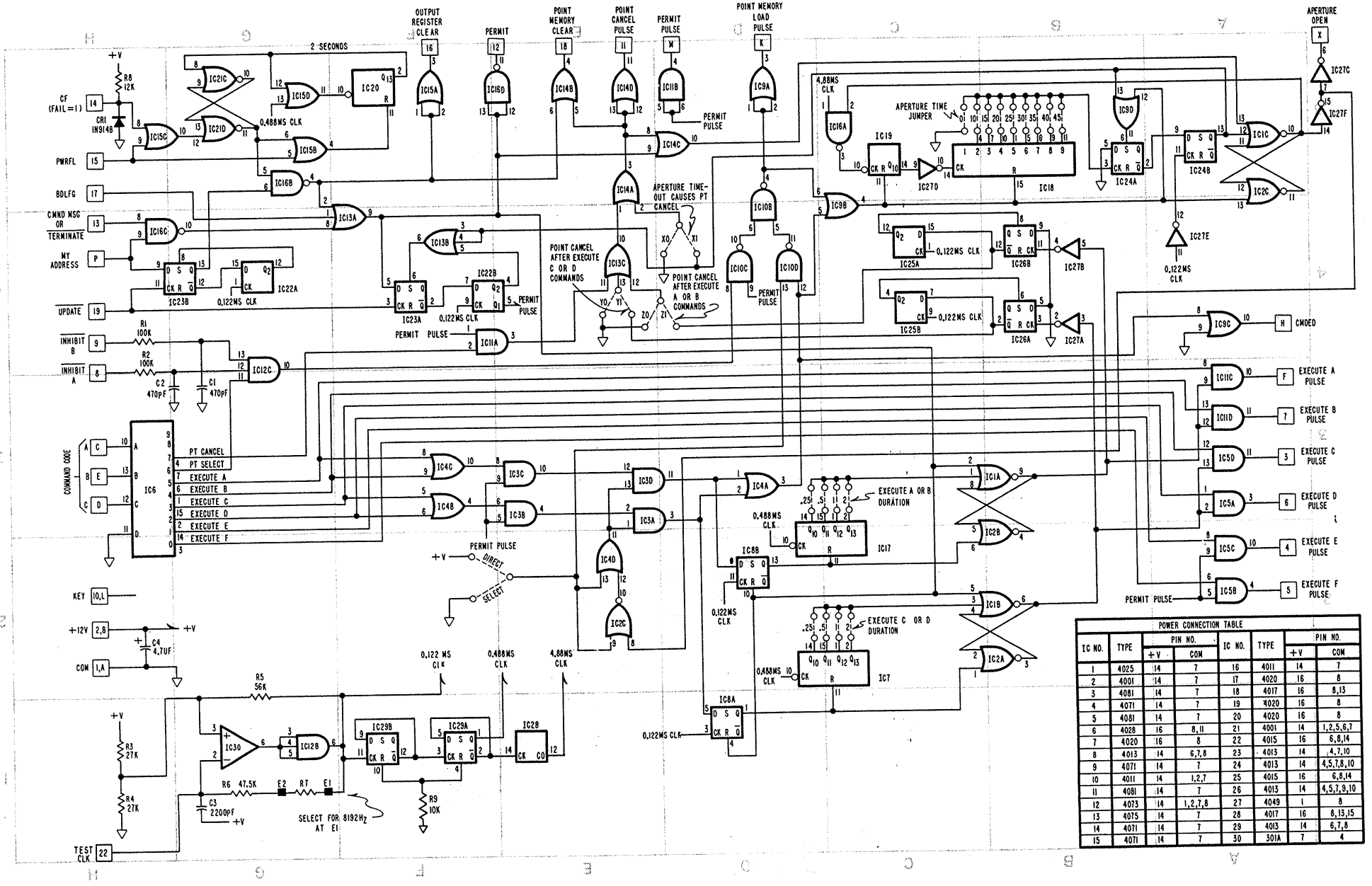
When the correct number of counts in IC17 has taken place, as determined by the EXECUTE DURATION Jumper (E3), IC1A-1 will go to a logic 1 and set the IC1A/IC2B flip-flop. The IC11C and IC11D gates are then closed.

At the end of the execute pulse, when IC1A-9 drops low, IC27B-4 (G2) will rise high and clock a one to IC26B-12 (F2). After two 0.122 mS pulses, IC26B will be set and IC26B-12 will drop low again. The pulse created at IC26B-12 may then be used if the Z1 Jumper (D2) is installed to cause a POINT CANCEL PULSE.

The EXECUTE DURATION and its ending pulse for the C and D commands functions similarly to the A and B action described above.

Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	RFL PART NO.
	Model 66 CMDEC Command Decoder, Assembly HB-44630	
C1, 2	Capacitor, ceramic 470pF, 10%, 100V, Union Carbide CK12BX471-K, or eq.	H-1007-1358
C3	Capacitor, ceramic 0.0022μF, 10%, 100V, Union Carbide CK12BX222-K, or eq.	H-1007-1368
C4	Capacitor, tantalum 4.7μF, 20%, 20V, Kemet T324B475M020AS, or eq.	H-1007-711
CR1	Diode, Type 1N914B	HA-26482
IC1	Triple, 3-input NOR gate, RCA CD4025AE, or eq.	H-0615-20
IC2, 21	Quad, 2-input NOR gate, RCA CD4001AE, or eq.	H-0615-3
IC3, 5, 11	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC4, 9, 14, 15	Quad, 2-input OR gate, RCA CD4071BE, or eq.	H-0615-24
IC6	BCD-to-decimal decoder, RCA CD4028AE, or eq.	H-0615-19
IC7, 17, 19, 20	14-stage ripple-carry binary counter/divider, RCA CD4020AE, or eq.	H-0615-2
IC8, 23, 24, 26, 29	Dual, D-type flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC10, 16	Quad, 2-input NAND gate, RCA CD4011AE, or eq.	H-0615-5
IC12	Triple, 3-input AND gate, RCA CD4073BE, or eq.	H-0615-32
IC13	Triple, 3-input OR gate, RCA CD4075BE, or eq.	H-0615-33
IC18, 28	Decade counter/divider, RCA CD4017AE, or eq.	H-0615-38
IC22, 25	Dual, 4-stage shift register, RCA CD4015AE, or eq.	H-0615-25
IC27	Hex inverter/buffer, RCA CD4049AE, or eq.	H-0615-7
IC30	Operational amplifier, National LM301AN, or eq.	H-0620-76
R1-6, 8, 9	Resistor, metal-film, precision, 1%, ¼W, value on schematic, Type RN¼ per RFL Spec HA-38328, or eq.	H-0410-(xxxx)
R7	Resistor, metal-film, 1%, 1/8W, value selected at factory, Type RN55D, RFL Spec HA-38301	H-1510-(xxx)
—	Shorting bar	HA-42904
—	Schematic	H-44634



POWER CONNECTION TABLE							
IC NO.	TYPE	PIN NO.		IC NO.	TYPE	PIN NO.	
		+V	COM			+V	COM
1	4025	14	7	16	4011	14	7
2	4001	14	7	17	4020	16	8
3	4081	14	7	18	4017	16	8,13
4	4071	14	7	19	4020	16	8
5	4081	14	7	20	4020	16	8
6	4028	16	8,11	21	4001	14	1,2,5,6,7
7	4020	16	8	22	4015	16	6,8,14
8	4013	14	6,7,8	23	4013	14	4,7,10
9	4071	14	7	24	4013	14	4,5,7,8,10
10	4011	14	1,2,7	25	4015	16	6,8,14
11	4081	14	7	26	4013	14	4,5,7,9,10
12	4073	14	1,2,7,8	27	4049	1	8
13	4075	14	7	28	4017	16	8,13,15
14	4071	14	7	29	4013	14	6,7,8
15	4071	14	7	30	301A	7	4

Figure 3. Schematic of Circuit, Model 66 CMDEC.